PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

#6/Election w/Attch A
R. Tyson
2/9/01

In re Application of:

Kinsman et al.

Serial No.: 09/538,684

Filed: March 30, 2000

For: VARIED-THICKNESS HEAT SINK FOR INTEGRATED CIRCUIT (IC) PACKAGES AND METHOD OF FABRICATING IC PACKAGES

Examiner: D. Graybill

Group Art Unit: 2814

Attorney Docket No.: 3056.1US (96-803.1)

CERTIFICATE OF MAILING

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Samuel E. Webb
Typed/printed name of person whose signature is contained above

AMENDMENT UNDER 37 C.F.R. § 1.111

Box Non-Fee Amendment
Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

This amendment is in response to the Election Of Species Restriction Requirement of January 3, 2001, having an initial period of response expiring on February 3, 2001.

IN THE CLAIMS:

Claims are presented below in format for publication.

Claims 1, 5, 9, 11, 13, 21-26, 30, 34 and 36 have been amended. Please enter these claims as amended.

Attached is Appendix A, which contains a marked-up version of the claims as revised.

1. (Amended) An integrated circuit (IC) package comprising:

a package body;

an IC die positioned within the package body;

a lead frame including a plurality of leads having portions enclosed within the package body that connect to the IC die; and

an electrically conductive heat sink positioned at least partially within the package body with a surface of a first portion of the heat sink facing the lead frame in close proximity to a substantial part of the enclosed portion of each of the plurality of leads of the lead frame and with a die-attach area on the surface of the first portion of the heat sink attached to the IC die, a second portion of the heat sink projecting away from the first portion of the heat sink under the die-attach area and the IC die.

2. The IC package of claim 1, wherein the package body is selected from a group comprising a transfer molded plastic package body and a preformed ceramic package body.

3. The IC package of claim 1, wherein the IC die is selected from a group comprising a Dynamic Random Access Memory (DRAM) IC die, a Static Random Access Memory (SRAM) IC die, a Synchronous DRAM (SDRAM) IC die, a Sequential Graphics Random Access Memory (SGRAM) IC die, a flash Electrically Erasable Programmable Read-Only Memory (EEPROM) IC die, and a processor IC die.

4. The IC package of claim 1, wherein the lead frame is selected from a group comprising a peripheral-lead finger lead frame, a Leads Over Chip (LOC) lead frame, and a Leads Under Chip (LUC) lead frame.

A2 5. (Amended) The IC package of claim 1, wherein the heat sink is coupled to one of a signal voltage and a reference voltage so the heat sink operates respectively as a signal plane and a ground plane for the plurality of leads of the lead frame.

NE 6. The IC package of claim 5, wherein the heat sink is coupled to the reference voltage through one of a wirebond, a conductive adhesive, and a welded connection.

7. The IC package of claim 1, wherein the heat sink is electrically isolated from the lead frame.

8. The IC package of claim 1, wherein the heat sink is positioned only partially within the package body.

A3 Sub B5 9. (Amended) The IC package of claim 1, wherein the heat sink is coupled to a printed circuit board outside the package body and is thereby coupled to one of a signal voltage and a reference voltage so the heat sink operates respectively as a signal plane and a ground plane for the plurality of leads of the lead frame.

10. The IC package of claim 8, wherein the second portion of the heat sink projects substantially to one of a top and a bottom of the package body.

A4 Sub B6 11. (Amended) The IC package of claim 1, wherein the heat sink is positioned within the package body with the surface of its first portion in close proximity to substantially all of the enclosed portion of each of the plurality of leads of the lead frame.

12. The IC package of claim 1, wherein the heat sink is positioned within the package body with its first portion extending substantially to at least one side of the package body.

13. (Amended) The IC package of claim 1, wherein the heat sink is positioned within the package body with the surface of its first portion in close proximity to at least eighty percent of an area of the enclosed portions of the plurality of leads of the lead frame.

14. The IC package of claim 1, wherein the first and second portions of the heat sink are integral with one another.

15. The IC package of claim 1, wherein the first and second portions of the heat sink comprise separate parts.

16. The IC package of claim 1, wherein the heat sink comprises a plurality of parts, each forming a portion of both the first and second portions of the heat sink.

17. The IC package of claim 1, wherein the surface of the first portion of the heat sink includes a recess in which the die-attach area is located.

18. The IC package of claim 1, wherein the heat sink has locking holes therein for locking the heat sink in the IC package.

19. The IC package of claim 1, further comprising an adhesive attaching the lead frame to the heat sink.

20. The IC package of claim 1, wherein the IC package comprises one of a Vertical Surface Mount Package (VSMP), a Small Outline J-lead (SOJ) package, a Thin Small Outline Package (TSOP), a Quad Flat Pack (QFP), and a Thin QFP (TQFP).

22. (Amended) An electronic system comprising an input device, an output device, a memory device, and a processor device coupled to the input, output, and memory devices, at least one of the input, output, memory, and processor devices including an integrated circuit (IC) package comprising:

a package body;

an IC die positioned within the package body;

a lead frame including a plurality of leads having portions enclosed within the package body that connect to the IC die; and

an electrically conductive heat sink positioned at least partially within the package body with a surface of a first portion of the heat sink facing the lead frame in close proximity to a substantial part of the enclosed portion of each of the plurality of leads of the lead frame and having a die-attach area on the surface of the first portion of the heat sink attached to the IC die, a second portion of the heat sink being opposite the die-attach area and projecting away from the first portion of the heat sink and the IC die.

23. (Amended) A lead frame assembly comprising:

a lead frame; and

a heat sink positioned with a surface thereof in a substantially mutually parallel and co-extensive relationship with, and in close but electrically insulated proximity to, the lead frame.

24. (Amended) An integrated circuit (IC) package comprising:

a package body;

an IC die positioned within the package body;

a lead frame including a plurality of leads having portions enclosed within the package body that connect to the IC die; and

an electrically conductive heat sink positioned at least partially within the package body with a vertically extending columnar portion surrounded by a horizontally extending skirt portion having a lead frame attachment surface proximate a die-attach surface substantially vertically aligned with the columnar portion, the lead frame attachment surface being attached to the lead frame and extending in close proximity to a substantial part of the enclosed portions of the plurality of leads of the lead frame, the die-attach surface being attached to the IC die.

25. (Amended) An integrated circuit (IC) package comprising:

an IC die;

a lead frame including a plurality of leads having portions that are connected to the IC die; and

an electrically conductive heat sink positioned having a surface of a first portion of the heat sink facing the lead frame in close proximity to a substantial part of an enclosed portion of each of the plurality of leads of the lead frame and with a die-attach area on the surface of the first portion of the heat sink attached to the IC die, a second portion of the heat sink projecting away from the first portion of the heat sink under the die-attach area and the IC die.

26. (Amended) The IC package of claim 25, further comprising a package body.

27. The IC package of claim 26, wherein the package body is selected from a group comprising a transfer molded plastic package body and a preformed ceramic package body.

28. The IC package of claim 25, wherein the IC die is selected from a group comprising a Dynamic Random Access Memory (DRAM) IC die, a Static Random Access Memory (SRAM) IC die, a Synchronous DRAM (SDRAM) IC die, a Sequential Graphics Random Access Memory (SGRAM) IC die, a flash Electrically Erasable Programmable Read-Only Memory (EEPROM) IC die, and a processor IC die.

29. The IC package of claim 25, wherein the lead frame is selected from a group comprising a peripheral-lead finger lead frame, a Leads Over Chip (LOC) lead frame, and a Leads Under Chip (LUC) lead frame.

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30. (Amended) The IC package of claim 25, wherein the heat sink is coupled to one of a signal voltage and a reference voltage so the heat sink operates respectively as a signal plane and a ground plane for the plurality of leads of the lead frame.

31. The IC package of claim 30, wherein the heat sink is coupled to the reference voltage through one of a wirebond, a conductive adhesive, and a welded connection.

32. The IC package of claim 25, wherein the heat sink is electrically isolated from the lead frame.

33. The IC package of claim 26, wherein the heat sink is positioned only partially within the package body.

A8 Sub 5/11

34. (Amended) The IC package of claim 26, wherein the heat sink is coupled to a printed circuit board outside the package body and is thereby coupled to one of a signal voltage and a reference voltage so the heat sink operates respectively as a signal plane and a ground plane for the plurality of leads of the lead frame.

35. The IC package of claim 34, wherein the second portion of the heat sink projects substantially to one of a top and a bottom of the package body.

A9 Sub 5/12

36. (Amended) The IC package of claim 26, wherein the heat sink is positioned within the package body with the surface of its first portion in close proximity to substantially all of the enclosed portion of each of the plurality of leads of the lead frame.

37. The IC package of claim 26, wherein the heat sink is positioned within the package body with its first portion extending substantially to at least one side of the package body.

38. The IC package of claim 26, wherein the heat sink is positioned within the package body with the surface of its first portion in close proximity to at least eighty percent of an area of the lead frame.

39. The IC package of claim 25, wherein the first and second portions of the heat sink are integral with one another.

40. The IC package of claim 25, wherein the first and second portions of the heat sink comprise separate parts.

41. The IC package of claim 25, wherein the heat sink comprises a plurality of parts, each forming a portion of both the first and second portions of the heat sink.

42. The IC package of claim 25, wherein the surface of the first portion of the heat sink includes a recess in which the die-attach area is located.

43. The IC package of claim 25, wherein the heat sink has locking holes therein for locking the heat sink in the IC package.

44. The IC package of claim 25, further comprising an adhesive attaching the lead frame to the heat sink.

45. The IC package of claim 25, wherein the IC package comprises one of a Vertical Surface Mount Package (VSMP), a Small Outline J-lead (SOJ) package, a Thin Small Outline Package (TSOP), a Quad Flat Pack (QFP), and a Thin QFP (TQFP).

REMARKS

Claims 1 through 45 are currently pending in the application and are subject to an Election of Species Restriction Requirement.

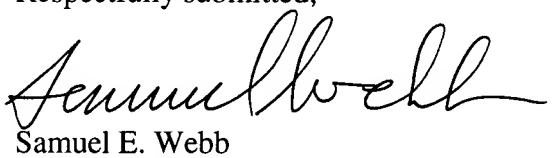
Applicants hereby elect, without traverse, to prosecute the species of invention as set forth in claims 1-6, 8-22, 24- 31, and 33- 45.

Applicants consider claims 1 and 25 to be generic.

Applicants request an action on the merits of claims 1-6, 8-22, 24- 31, and 33- 45.

If the Examiner has any questions regarding Applicants' election, he is respectfully invited to contact Applicants' attorney at the telephone number provided.

Respectfully submitted,



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